# Computer Architecture

## Tutorial 5

## John Sinclair 16325734

Q1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **128 byte 1-way cache with 16 bytes per line (direct mapped) –> 3 set bits** | | | | | |
| **Hex** | **Binary** | **Offset** | **Set** | **Tag** | **Hit** |
| 0000 | 0000 0000 0000 0000 | 0000 | 000 | 0000 0000 0 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 000 | 0000 0000 0 | Yes |
| 000c | 0000 0000 0000 1100 | 1100 | 000 | 0000 0000 0 | Yes |
| 00d0 | 0000 0000 1101 0000 | 0000 | 101 | 0000 0000 1 |  |
| 00e0 | 0000 0000 1110 0000 | 0000 | 110 | 0000 0000 1 |  |
| 1130 | 0001 0001 0011 0000 | 0000 | 011 | 0001 0001 0 |  |
| 0028 | 0000 0000 0010 1000 | 1000 | 010 | 0000 0000 0 |  |
| 113c | 0001 0001 0011 1100 | 1100 | 011 | 0001 0001 0 | Yes |
| 2204 | 0010 0010 0000 0100 | 0100 | 000 | 0010 0010 0 |  |
| 0010 | 0000 0000 0001 0000 | 0000 | 001 | 0000 0000 0 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 000 | 0000 0000 0 |  |
| 0040 | 0000 0000 0100 0000 | 0000 | 100 | 0000 0000 0 |  |
| 2208 | 0010 0010 0000 1000 | 1000 | 000 | 0010 0010 0 |  |
| 0008 | 0000 0000 0000 1000 | 1000 | 000 | 0000 0000 0 |  |
| 00a0 | 0000 0000 1010 0000 | 0000 | 010 | 0000 0000 1 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 000 | 0000 0000 0 | Yes |
| 1104 | 0001 0001 0000 0100 | 0100 | 000 | 0001 0001 0 |  |
| 000c | 0000 0000 0000 1100 | 0100 | 000 | 0000 0000 0 |  |
| 0084 | 0000 0000 1000 0100 | 0100 | 000 | 0000 0000 1 |  |
| 000c | 0000 0000 0000 1100 | 1100 | 000 | 0000 0000 0 |  |
| 3390 | 0011 0011 1001 0000 | 0000 | 001 | 0011 0011 1 |  |
| 00b0 | 0000 0000 1011 0000 | 0000 | 011 | 0000 0000 1 |  |
| 1100 | 0001 0001 0000 0000 | 0000 | 000 | 0001 0001 0 |  |
| 0028 | 0000 0000 0010 1000 | 1000 | 010 | 0000 0000 0 |  |
| 0070 | 0000 0000 0111 0000 | 0000 | 111 | 0000 0000 0 |  |
| 00d0 | 0000 0000 1101 0000 | 0000 | 101 | 0000 0000 1 | Yes |
| 0008 | 0000 0000 0000 1000 | 1000 | 000 | 0000 0000 0 |  |
| 3394 | 0011 0011 1001 0100 | 0100 | 001 | 0011 0011 1 | Yes |

Hits: 6

Misses: 22

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **128 byte 2-way set associative cache with 16 bytes per line –> 2 set bits** | | | | | |
| **Hex** | **Binary** | **Offset** | **Set** | **Tag** | **Hit** |
| 0000 | 0000 0000 0000 0000 | 0000 | 00 | 0000 0000 00 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 00 | 0000 0000 00 | Yes |
| 000c | 0000 0000 0000 1100 | 1100 | 00 | 0000 0000 00 | Yes |
| 00d0 | 0000 0000 1101 0000 | 0000 | 01 | 0000 0000 11 |  |
| 00e0 | 0000 0000 1110 0000 | 0000 | 10 | 0000 0000 11 |  |
| 1130 | 0001 0001 0011 0000 | 0000 | 11 | 0001 0001 00 |  |
| 0028 | 0000 0000 0010 1000 | 1000 | 10 | 0000 0000 00 |  |
| 113c | 0001 0001 0011 1100 | 1100 | 11 | 0001 0001 00 | Yes |
| 2204 | 0010 0010 0000 0100 | 0100 | 00 | 0010 0010 00 |  |
| 0010 | 0000 0000 0001 0000 | 0000 | 01 | 0000 0000 00 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 00 | 0000 0000 00 | Yes |
| 0040 | 0000 0000 0100 0000 | 0000 | 00 | 0000 0000 01 |  |
| 2208 | 0010 0010 0000 1000 | 1000 | 00 | 0010 0010 00 |  |
| 0008 | 0000 0000 0000 1000 | 1000 | 00 | 0000 0000 00 |  |
| 00a0 | 0000 0000 1010 0000 | 0000 | 10 | 0000 0000 10 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 00 | 0000 0000 00 | Yes |
| 1104 | 0001 0001 0000 0100 | 0100 | 00 | 0001 0001 00 |  |
| 000c | 0000 0000 0000 1100 | 0100 | 00 | 0000 0000 00 | Yes |
| 0084 | 0000 0000 1000 0100 | 0100 | 00 | 0000 0000 10 |  |
| 000c | 0000 0000 0000 1100 | 1100 | 00 | 0000 0000 00 | Yes |
| 3390 | 0011 0011 1001 0000 | 0000 | 01 | 0011 0011 10 |  |
| 00b0 | 0000 0000 1011 0000 | 0000 | 11 | 0000 0000 10 |  |
| 1100 | 0001 0001 0000 0000 | 0000 | 00 | 0001 0001 00 |  |
| 0028 | 0000 0000 0010 1000 | 1000 | 10 | 0000 0000 00 | Yes |
| 0070 | 0000 0000 0111 0000 | 0000 | 11 | 0000 0000 01 |  |
| 00d0 | 0000 0000 1101 0000 | 0000 | 01 | 0000 0000 11 |  |
| 0008 | 0000 0000 0000 1000 | 1000 | 00 | 0000 0000 00 | Yes |
| 3394 | 0011 0011 1001 0100 | 0100 | 01 | 0011 0011 10 | Yes |

Hits: 10

Misses: 18

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **128 byte 4-way set associative cache with 16 bytes per line –> 1 set bit** | | | | | |
| **Hex** | **Binary** | **Offset** | **Set** | **Tag** | **Hit** |
| 0000 | 0000 0000 0000 0000 | 0000 | 0 | 0000 0000 000 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 0 | 0000 0000 000 | Yes |
| 000c | 0000 0000 0000 1100 | 1100 | 0 | 0000 0000 000 | Yes |
| 00d0 | 0000 0000 1101 0000 | 0000 | 1 | 0000 0000 110 |  |
| 00e0 | 0000 0000 1110 0000 | 0000 | 0 | 0000 0000 111 |  |
| 1130 | 0001 0001 0011 0000 | 0000 | 1 | 0001 0001 001 |  |
| 0028 | 0000 0000 0010 1000 | 1000 | 0 | 0000 0000 001 |  |
| 113c | 0001 0001 0011 1100 | 1100 | 1 | 0001 0001 001 | Yes |
| 2204 | 0010 0010 0000 0100 | 0100 | 0 | 0010 0010 000 |  |
| 0010 | 0000 0000 0001 0000 | 0000 | 1 | 0000 0000 000 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 0 | 0000 0000 000 | Yes |
| 0040 | 0000 0000 0100 0000 | 0000 | 0 | 0000 0000 010 |  |
| 2208 | 0010 0010 0000 1000 | 1000 | 0 | 0010 0010 000 | Yes |
| 0008 | 0000 0000 0000 1000 | 1000 | 0 | 0000 0000 000 | Yes |
| 00a0 | 0000 0000 1010 0000 | 0000 | 0 | 0000 0000 101 |  |
| 0004 | 0000 0000 0000 0100 | 0100 | 0 | 0000 0000 000 | Yes |
| 1104 | 0001 0001 0000 0100 | 0100 | 0 | 0001 0001 000 |  |
| 000c | 0000 0000 0000 1100 | 0100 | 0 | 0000 0000 000 | Yes |
| 0084 | 0000 0000 1000 0100 | 0100 | 0 | 0000 0000 100 |  |
| 000c | 0000 0000 0000 1100 | 1100 | 0 | 0000 0000 000 | Yes |
| 3390 | 0011 0011 1001 0000 | 0000 | 1 | 0011 0011 100 |  |
| 00b0 | 0000 0000 1011 0000 | 0000 | 1 | 0000 0000 101 |  |
| 1100 | 0001 0001 0000 0000 | 0000 | 0 | 0001 0001 000 | Yes |
| 0028 | 0000 0000 0010 1000 | 1000 | 0 | 0000 0000 001 |  |
| 0070 | 0000 0000 0111 0000 | 0000 | 1 | 0000 0000 011 |  |
| 00d0 | 0000 0000 1101 0000 | 0000 | 1 | 0000 0000 110 |  |
| 0008 | 0000 0000 0000 1000 | 1000 | 0 | 0000 0000 000 | Yes |
| 3394 | 0011 0011 1001 0100 | 0100 | 1 | 0011 0011 100 | Yes |

Hits: 12

Misses: 16

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **128 byte 8-way associative cache with 16 bytes per line (fully associative) –> 0 set bits** | | | | | |
| **Hex** | **Binary** | **Offset** | **Set** | **Tag** | **Hit** |
| 0000 | 0000 0000 0000 0000 | 0000 |  | 0000 0000 0000 |  |
| 0004 | 0000 0000 0000 0100 | 0100 |  | 0000 0000 0000 | Yes |
| 000c | 0000 0000 0000 1100 | 1100 |  | 0000 0000 0000 | Yes |
| 00d0 | 0000 0000 1101 0000 | 0000 |  | 0000 0000 1101 |  |
| 00e0 | 0000 0000 1110 0000 | 0000 |  | 0000 0000 1110 |  |
| 1130 | 0001 0001 0011 0000 | 0000 |  | 0001 0001 0011 |  |
| 0028 | 0000 0000 0010 1000 | 1000 |  | 0000 0000 0010 |  |
| 113c | 0001 0001 0011 1100 | 1100 |  | 0001 0001 0011 | Yes |
| 2204 | 0010 0010 0000 0100 | 0100 |  | 0010 0010 0000 |  |
| 0010 | 0000 0000 0001 0000 | 0000 |  | 0000 0000 0001 |  |
| 0004 | 0000 0000 0000 0100 | 0100 |  | 0000 0000 0000 | Yes |
| 0040 | 0000 0000 0100 0000 | 0000 |  | 0000 0000 0100 |  |
| 2208 | 0010 0010 0000 1000 | 1000 |  | 0010 0010 0000 | Yes |
| 0008 | 0000 0000 0000 1000 | 1000 |  | 0000 0000 0000 | Yes |
| 00a0 | 0000 0000 1010 0000 | 0000 |  | 0000 0000 1010 |  |
| 0004 | 0000 0000 0000 0100 | 0100 |  | 0000 0000 0000 | Yes |
| 1104 | 0001 0001 0000 0100 | 0100 |  | 0001 0001 0000 |  |
| 000c | 0000 0000 0000 1100 | 0100 |  | 0000 0000 0000 | Yes |
| 0084 | 0000 0000 1000 0100 | 0100 |  | 0000 0000 1000 | Yes |
| 000c | 0000 0000 0000 1100 | 1100 |  | 0000 0000 0000 | Yes |
| 3390 | 0011 0011 1001 0000 | 0000 |  | 0011 0011 1001 |  |
| 00b0 | 0000 0000 1011 0000 | 0000 |  | 0000 0000 1011 |  |
| 1100 | 0001 0001 0000 0000 | 0000 |  | 0001 0001 0000 | Yes |
| 0028 | 0000 0000 0010 1000 | 1000 |  | 0000 0000 0010 |  |
| 0070 | 0000 0000 0111 0000 | 0000 |  | 0000 0000 0111 |  |
| 00d0 | 0000 0000 1101 0000 | 0000 |  | 0000 0000 1101 |  |
| 0008 | 0000 0000 0000 1000 | 1000 |  | 0000 0000 0000 | Yes |
| 3394 | 0011 0011 1001 0100 | 0100 |  | 0011 0011 1001 | Yes |

Hits: 13

Misses: 15

Q2

Instruction cache miss rate = 2%

Data cache miss rate = 4%

CPI = 2

Miss penalty = 100

36% of instructions are load/ stores

Instruction miss cycles = number of instructions \* 2% \* 100 = 2(number of instructions)

Data miss cycles = number of instructions \* 36% \*4% \* 100 = 1.44(no. of instructions)

Total memory stall cycles = 2 + 1.44 = 3.44

CPU execution time per instruction = 3.44 + 2 = 5.44

(CPU time with stalls / CPU time with perfect cache) = (5.44 / 2) = 2.72

Therefore, a system with a perfect cache would be able to run 2.72 times faster than our imperfect one.

Q3

1. 2.5 ns – time needed to determine whether cache miss has occurred.

The line is then read into the cache, we have 16 words (64 bytes / 4 bytes), the first of which takes 50 ns to access and the remaining 15 cost 5 ns per word.

An additional 2.5 ns required to access the word.

Access time for cache miss = 2.5 + 50 + ((60 / 4) \* 5) + 2.5 = 130 ns

1. Average access time = (0.95 \* 2.5) + (0.05 \* 130) = 9.875 ns

New access time for cache miss = 2.5 + 50 + ((124 / 4) \* 5) + 2.5 = 210 ns

New average access time = (0.97 \* 2.5) + (0.03 \* 210) = 8.725 ns

Increasing the line size from 64 to 128 bytes reduces the average memory access time by 0.15 ns.

Q4

Miss Penalty formula:

Miss penalty = cache line size \* (clock cycle to send address to main memory + clock cycles to access a 32-bit)

1. Miss penalty = 1 \* (1 + 4) = 5
2. Miss penalty = 4 \* (1 + 4) = 20
3. Miss penalty = first word at (1 + 4) clock cycles, then remaining 3 words at (1 + 0) clock cycles (1 \* (1 + 4)) + (3 \* (1 + 0)) = 8